AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A method of simulating a circuit, comprising the steps of:

identifying a set of logic events associated with said circuit, wherein the logic events are represented as data objects embodying logic equations;

generating a plurality of input test cases;

simulating operation of said circuit utilizing said plurality of input test cases;

tabulating for the plurality of input test cases and the set of logic events the numbers of times that each input test case stimulates each logic event[[s]]; and

identifying as non-occurring events one or more logic events that have not been stimulated more than a predetermined threshold of times ~~as non-occurring events~~.

2. (Original) The method of claim 1 further comprising the steps of:

selecting one event of said non-occurring events; and

comparing a logic equation of said one event against logic equations of logic events that have been stimulated more than a predetermined threshold.

3. (Original) The method of claim 2 wherein the step of comparing comprises the sub-step of:

assigning scores to compared events, wherein said scores reflect similarity to said one event.

4. (Original) The method of claim 3 further comprising the step of:

utilizing said scores and said numbers of times to weight instructions contained in said input test cases.

5. (Original) The method of claim 4 further comprising the step of:

constructing a new test case from said weighted instructions.

6. (Original) The method of claim 5 wherein each test case possesses a plurality of instructions with each instruction respectively associated with generation strides.

7. (Original) The method of claim 6 wherein the generation strides are relatively prime.

8. (Original) The method of claim 5 wherein the step of tabulating comprises the sub-step of:

recording numbers of times in a matrix.

9. (Original) The method of claim 7 wherein the step of construction comprises the sub-step of:

assigning heavily weighted instructions to lower strides.

10. (Original) The method of claim 7 wherein the step of construction comprises the sub-step of:

weighting strides associated with particular instructions.

11. (Currently Amended) A system for simulating, comprising:

a data structure including a set of logic events associated with said circuit, wherein the logic events are represented as data objects embodying logic equations;

a first software routine generating a plurality of input test cases;

a second software routine applying said plurality of input test cases to a circuit simulator;

a third software routine tabulating for the plurality of input test cases and the set of logic events the numbers of times that each input test case stimulates each logic event[[s]]; and

a fourth software routine identifying as non-occurring events one or more logic events that have not been stimulated more than a predetermined threshold of times ~~as non-occurring events~~.

12. (Original) The system of claim 11 further comprising:

a fifth software routine selecting one event of said non-occurring events; and

a sixth software routine comparing a logic equation of said one event against logic equations of logic events that have been simulated more than a predetermined threshold.

13. (Original) The system of claim 12 wherein said sixth software routine assigns scores to compared events, wherein said scores reflect similarity to said one event.

14. (Original) The system of claim 13 further comprising:

a seventh software routine utilizing said scores and said numbers of times to weight instructions contained in said input test cases.

15. (Original) The system of claim 14 further comprising:

an eighth software routine constructing a new test case from said weighted instructions.

16. (Original) The system of claim 15 wherein each test case possesses a plurality of instructions with each instruction respectively associated with generation strides.

17. (Original) The system of claim 16 wherein the generation strides are relatively prime.

18. (Original) The system of claim 15 wherein the third software routine records numbers of times in a matrix.

19. (Currently Amended) A computer program product having a computer readable medium having programmable logic recorded thereon for testing a circuit, the computer product comprising:

means for representing a set of logic events associated with said circuit as data objects embodying logic equations;

means for generating a plurality of input test cases for application to a circuit simulator;

means for tabulating for the plurality of input test cases and the set of logic events the numbers of times that each input test case stimulates each logic event[[s]];

means for identifying as non-occurring events one or more logic events that have not been stimulated more than a predetermined threshold of times ~~as non-occurring events~~;

means for selecting one event of said non-occurring events; and

means for comparing a logic equation of said one event against logic equations of logic events that have been simulated more than a predetermined threshold.

20. (Original) A computer program product of claim 19 further comprising:

means for weighting instructions contained in said input test cases utilizing output from said means for comparing and said numbers of times; and

means for constructing a new test case from said weighted instructions.